CubeSat: Payload Electronics for Phased-Array Fed Lens Antennas

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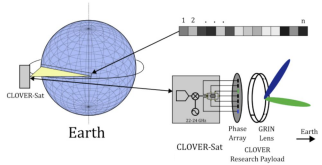
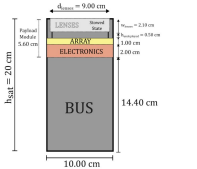
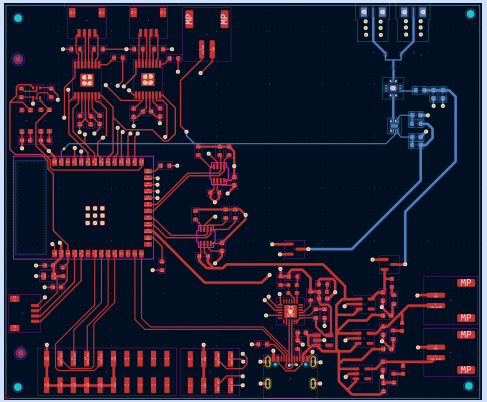
Background

The student design team IrishSat's CLOVER-Sat mission is a 2U CubeSat mission intended to carry a payload in collaboration with Dr. Jonathan Chisum. The payload will be a low-power, low-cost millimeter wave (MMW) phased-array fed gradient index lens (PAFL) antenna receiver operating in the K-band (~23.8 GHz) for Earth downlink communications and Earth science missions. This project aims to develop the first iteration of the electronics necessary for the PAFL payload structure to operate and interface with the rest of the CLOVER-Sat system.





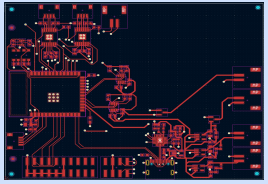
Main Board



4-Layer Board Layout

DC
- USB power supply and interface with host computer
- One +3.3V voltage regulator to supply VDD
- Three +4V voltage regulators to supply low-noise amplifiers
- ESP32-S3-WROOM-1 microcontroller
- Connection interface to beamformer evaluation board, for SPI communication
- Power tracking circuit for lines to RF side
- Power MOSFET circuits to execute low power mode
- Motor control drivers and external connection interface
- Breakout connection point for I2C communication with IrishSat flight computer

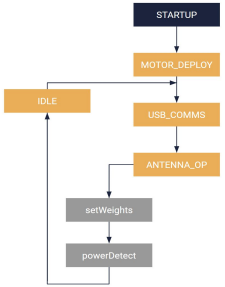
RF
- 2 input channels taking in RF signals from beamformer
- T-junction to combine power from horizontally and vertically polarized inputs
- Low-noise amplifier to increase RF signal gain
- Power detector to translate RF signal into DC voltage value for interpretation



2-Layer Board Layout

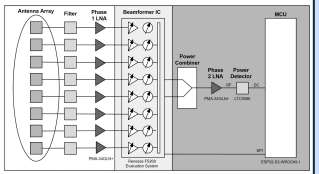
Software Architecture

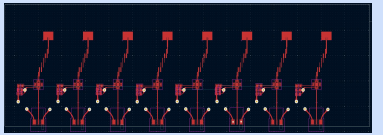
- State machine architecture designed to run through operations necessary for the intended CubeSat mission
- **STARTUP**
- **MOTOR_DEPLOY** sets up the motor speed and desired lambda, actuates the motors, and determines the actual motor position
- **USB_COMMS**
- **ANTENNA_OP** sets the weights on the antennas using SPI, reads out from the power detector, and outputs a visualization of the results
- **IDLE** is the base state Where the system waits for new comms



Payload Electronics

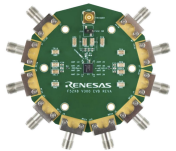
Antennas
- We milled an antenna board that consists of 8 patch antennas and filters, designed to operate around 23.8 GHz
- After passing through the filters, RF signals reach their first phase of amplification through 8 low-noise amplifiers, powered through +4V lines
- Our horn antenna test system consists of 4 horn antennas receiving an input signal at 23.8 GHz
- Signals are passed through RF coaxial connectors to the BFIC inputs





Antenna Board Layout

Beamformer IC Evaluation Board
- The BFIC eval. board allows the F5268 chip to interface with 8 RF inputs & 2 RF outputs, as well as connect directly to a digital interface for SPI communication purposes
- All 8 inputs come in from the antenna board, are magnitude amplified and/or phase shifted by the BFIC, and are power combined into 2 RF outputs before reaching the main board
- This was selected for this iteration as it was supplied to the project by Renesas and eliminated significant complexity and expense in mounting



System Requirements

- Supply voltage at +3.3V and +4V for DC and RF chips
- Electrical control to deploy lens using stepper motors to a set F/d
- Track power consumption from RF components & be able to enter low power mode
- Use SPI communication to set beamformer magnitude and phase weights using weight table determined using particle swarm algorithm
- Detect power of incoming signal centered at 23.8 GHz
- Develop test rig, complete with beam scanning simulation and display of results on host computer

Future Developments

- Integrate full system into 1 compact PCB with higher quality, space grade parts
- Implement an I/Q demodulator and linear oscillator to demodulate in phase and out of phase signals
- Develop an antenna calibration mechanism, i.e. looking into deep space and determining the power read out
- Extend the antenna array to multiple dimensions